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Circuit simulation of adaptive resonance theory (ART) neural network using Pspice

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This paper outlines the design and simulation of an analogue integrated circuit for the adaptive resonanace theory (ART1) neural network. The circuit is designed based on a set of coupled differential equations which describe the behaviour of the neural network and on analogue electronic components such as operational amplifiers. It performs the same functionality as the one-node neural network in the F2 layer of ART1. We have implemented and verified the circuit using a circuit simulator called Pspice run on a SPARC II Sun workstation. Results obtained from circuit simulation compare favourably with those calculated directly from the coupled differential equations. The one-node circuit developed here can be used as a subcircuit for a larger ART1 neural network with an arbitrary number of nodes.

1. Introduction

There are two prominent adaptive resonance theory (ART) neural network architectures: the ART1 and the ART2 (Grossberg 1988). Both architectures are capble in classifying an arbitrary set of input patterns into different categories. The categories are formed based on the similarities of the input patterns presented to the network. The ART1 was derived by Carpenter and Grossberg (1987), and classifies an arbitrary set of binary input patterns into different categories. It consists of two layers of nodes denoted by F1 and F2 (see Fig. 1). The nodes in the F1 layer are

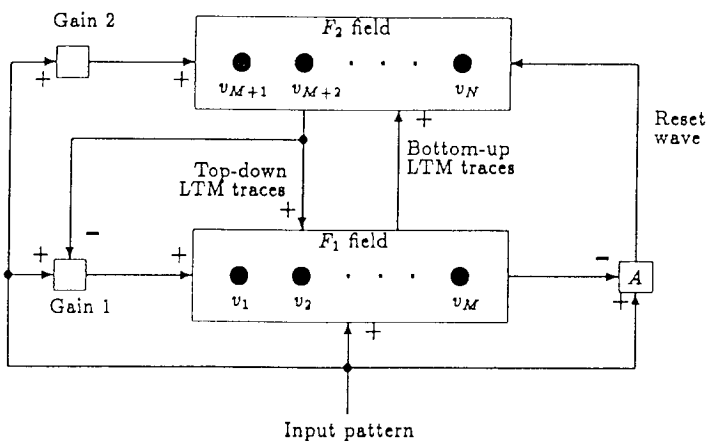

Figure 1. The architecture of the ART1 neural network which consists of the F1 and F2 layers.

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completely interconnected with the nodes in the F2 layers, and vice versa. Furthermore, the nodes in the F2 layer are completely interconnected with each other. The ART1 can only respond to binary inputs whereas the ART2 can respond to binary as well as analogue inputs. One of the advantages of the ART1 architecture is its ability to perform in real-time or on-line (without requiring external control or supervision) when it is implemented in hardware (Tsay and Newcomb 1991, Maher *et al.* 1989).

In this paper we design an analogue integrated circuit for the one-node F2 layer ART1 neural network. If proven functional, the circuit can be used as a subcircuit for a larger ART1 neural network incorporating both F1 and F2 layers in conjunction with their interconnections. Our circuit design is based on operational amplifiers which are relatively inexpensive and have been widely used in many circuit applications (Reed and Geiger 1989). The circuits designed will be verified using Pspice, a circuit simulator run on a Sun workstation. Comparisons will also be made between the Pspice simulations and the results obtained from solving the differential equations.

2. Background

The binary ART1 neural network is a two-field nearest neighbour classifier that stores an arbitrary number of binary input patterns, $I_k=(I_1^k, \ldots, K_n^k)$, $k=1, \ldots, m$, using competitive learning. ART1 learns on-line, operates in discrete or continuous time and has the topology shown in Fig. 1. From Fig. 1, we can see that ART1 consists of two major subsystems: the attentional and orienting subsystems. The F1 and F2 fields in the attentional subsystem consists of a single layer of nodes. These nodes are used to encode patterns of short term memory (STM) activity, while the weighted connections between the nodes in the F1 and F2 layers are used to store long term memory (LTM) traces. Each node in the F1 field is connected via bottom-up connections to all the nodes in the F2 field, and each node in the F2 field is connected via top-down connections to each of the F1 field nodes. In addition, the set of nodes comprising the F2 field are completely connected. The orienting system, A, receives input from the F1 field nodes, as well as from the input pattern. This subsystem will generate a reset wave to the F2 field whenever the input pattern is not matched close enough to the pattern of STM activity across the F1 field.

Hardware implementation of ART1 is very desirable because we can then take complete advantage of the parallel processing capabilities to achieve real-time processing speeds (Habib and Akel 1989), and the circuit developed here is suited for that purpose.

3. Circuit design and simulation

We focus on the one-node neural network in the F2 layer of the ART1. Figure 2 shows the block diagram of such a neural network. The inputs of the network are $-$T5 and F2(X6). The notations I, +, X, S and F2 denote the inverter, the summer, the multiplier, the integrator, and the comparator cells, respectively. In the block diagram, the derivative of X5 is fed into an inverting integrator which has a unity RC time constant. Then, $-$X5 is inverted to form the output X5. This signal is then fed into the multipliers and the summer. The F2(X5) comparator checks the state of the differential voltage of the feedback loop. This comparator outputs zero voltage until a present threshold voltage is reached, then the comparator outputs a constant

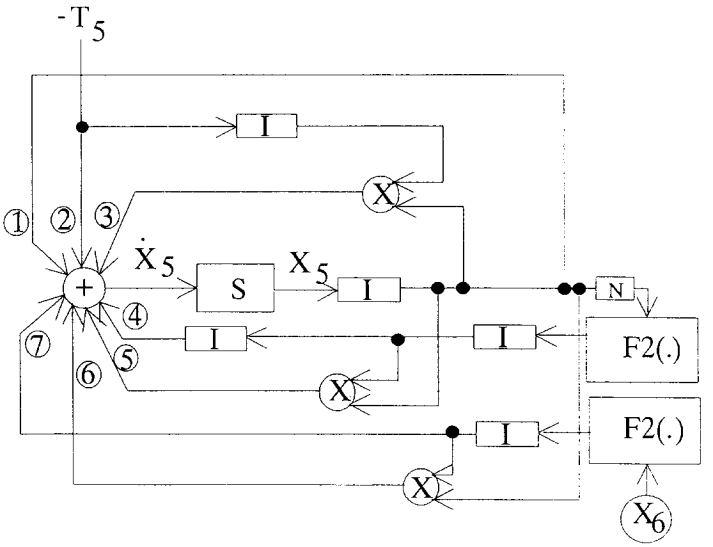
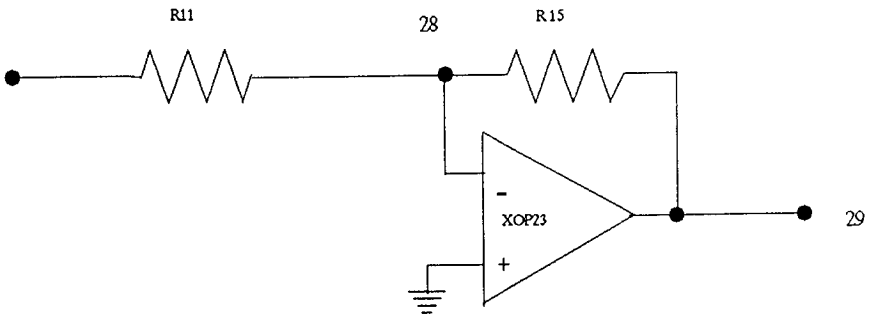


Figure 2. Block diagram of the F2 layer of ART1.

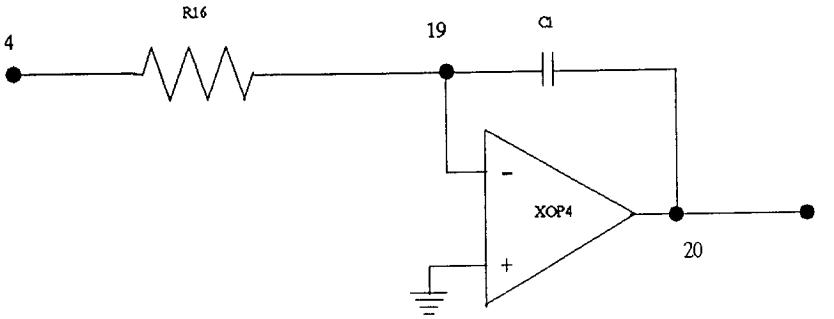
voltage. The F2(X6) comparator senses the input from the X6 node and performs similarly to the F2(X5) comparator. All of the outputs are then fed back into an inverting summer.

We have designed all the cells (inverter, multiplier, comparator, etc). based on operational amplifiers which have been widely used in many circuit applications and are relatively inexpensive. The circuits for the inverter, integrator, multiplier and comparator cells are given in Figs 3(*a*)-(*d*), respectively, in which the operational amplifiers are represented by a triangle having two input nodes and one output node. All cells have been optimized and verified using a circuit simulator called Pspice, which is a Sun workstation version of SPICE developed by MicroSim Corp.

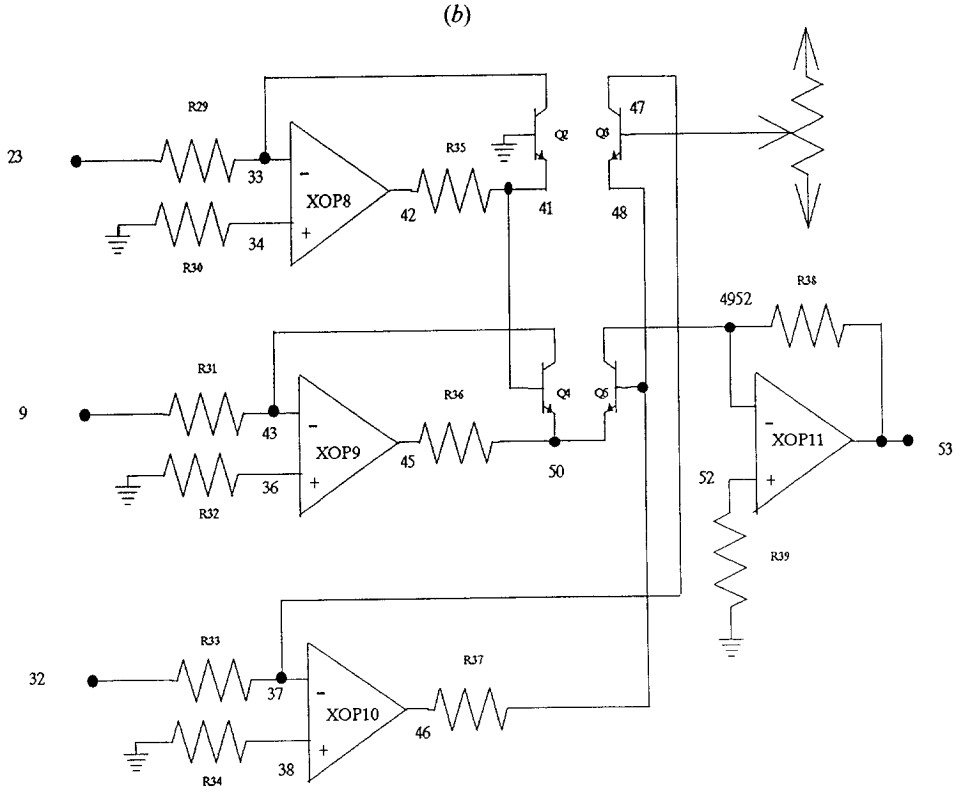
Two different simulation methods are available in Pspice. The first method considers the actual circuit components and models these components using subcircuits provided in the Pspice library. In the course of our simulations, the OP-27 operational-amplifier subcircuit available in the Pspice library has been shown to yield the best accuracy and thus has been chosen to model the operational amplifiers. We call this method circuit component modelling. The other method is to simulate the circuit using an option in Pspice called analogue behavioural modelling. This feature allows for flexible descriptions of circuit components in terms of mathematical functions. This option is a built-in extension to the intrinsic voltage-controlled voltage source and the voltage-controlled current source in Pspice. Note that while the analogue behavioural modelling is less realistic compared with the circuit component modelling, it has a distinct advantage on the speed of circuit simulation. Since the cell circuits are relatively simple, their simulations are carried out using circuit component modelling. The simulated results of the comparator cell developed (Fig. 3(*d*), which has a threshold voltage of 0 V, are illustrated in Fig. 4. The results show that the cell performs as desired; it outputs zero when the input signal is smaller than the threshold voltage and outputs a constant voltage (1 V for



(a)



(b)



(c)

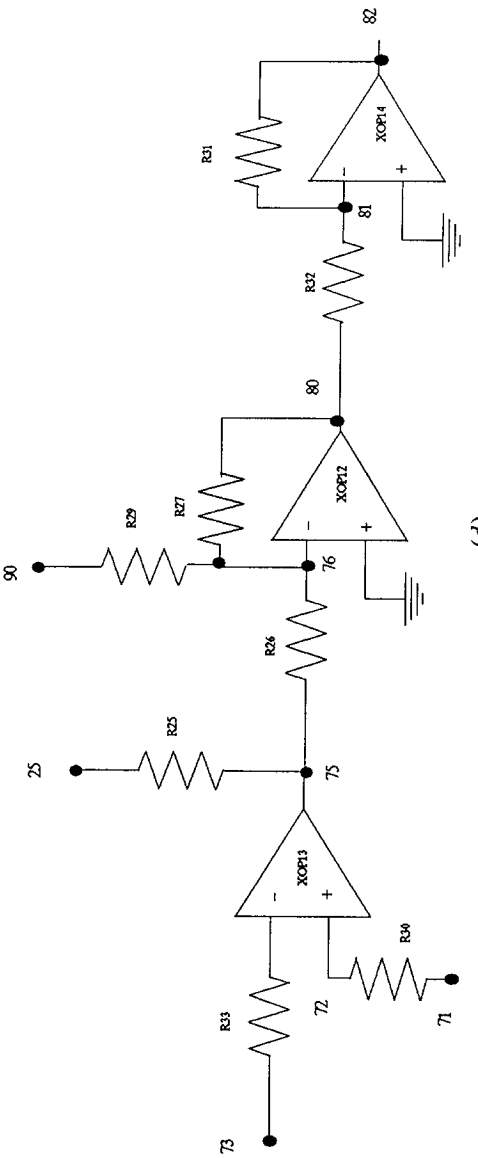


Figure 3. Circuit representations of (*a*) inverter cell; (*b*) integrator cell; (*c*) multiplier cell; and (*d*) comparator cell.

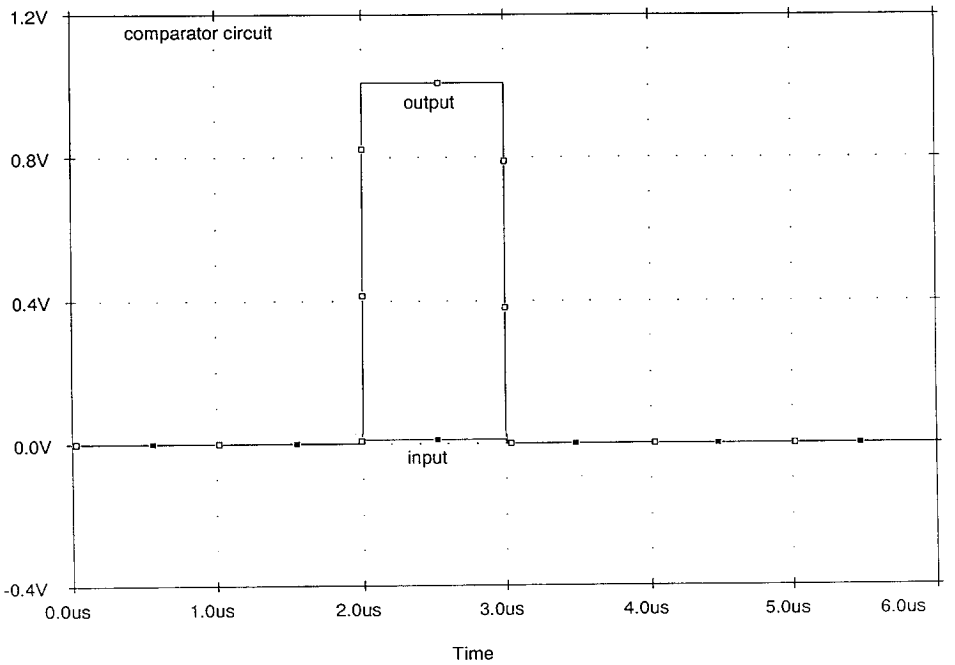


Figure 4. Pspice circuit simulation results of the comparator having a threshold voltage of 0 V subjected to a step input signal.

this case) when the input signal is larger (0·001 V) for this case) than the threshold voltage.

The cells are then connected according to the block diagram (Fig. 2) to form the complete integrated circuit for the one-node neural network, which is shown in Fig. 5. To predict and verify the circuit, we again carry out Pspice circuit simulations. Because this circuit is much more complex than the cell circuit, we employ circuit component modelling as well as analogue behavioural modelling, which replaces the complicated cells like the multipliers and comparators by mathematical functions represented by the blocks in Fig. 6. The latter approach reduces the simulation time drastically; circuit simulations on a SPARC II Sun workstation using the circuit component modelling take about two and half hours to run and more than 1 MB of RAM, whereas the behavioural modelling aproach simulates the circuit in about three seconds and uses less than 5 kB of RAM.

Comparisons of the results for the one-node F2 layer ART1 neural network simulated from the circuit component modelling (dashed lines), the analogue behavioural modelling (solid line), and the exact coupled differential equation (dotted lines) are given in Fig. 7. Excellent agreement is obtained between the analogue behavioural modelling and the exact solution. Some discrepancies are found associated with the circuit component modelling, which result from the non-ideal behaviour of the actual circuit components.

The one-node neural network integrated circuit developed here can be used as a subcircuit for a larger ART1 neural network with an arbitrary number of nodes. For example, a two-node ART1 neural network can be constructed using the one-node

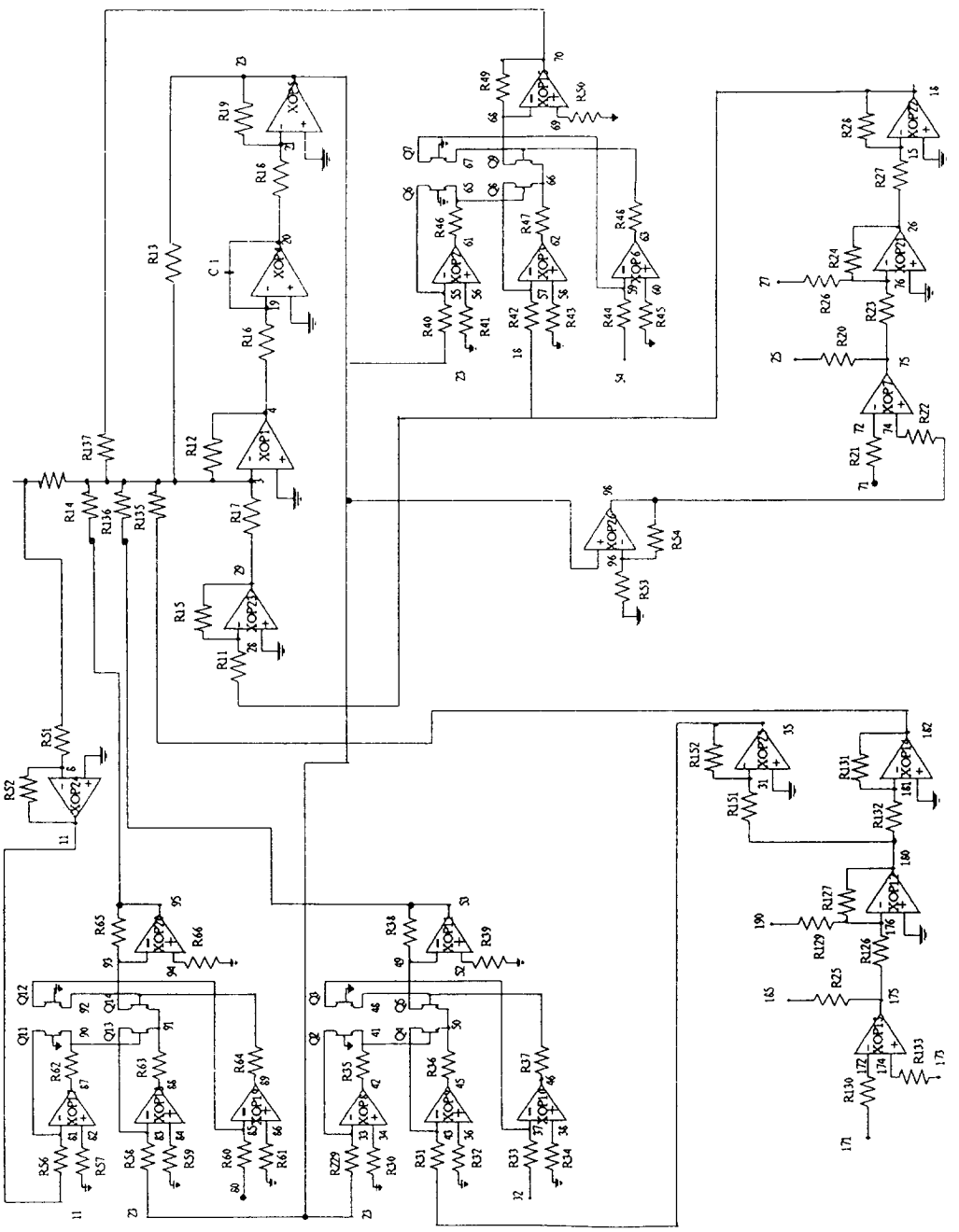


Figure 5. Integrated circuit designed for the one-node neural network in the F2 layer of the ART1.

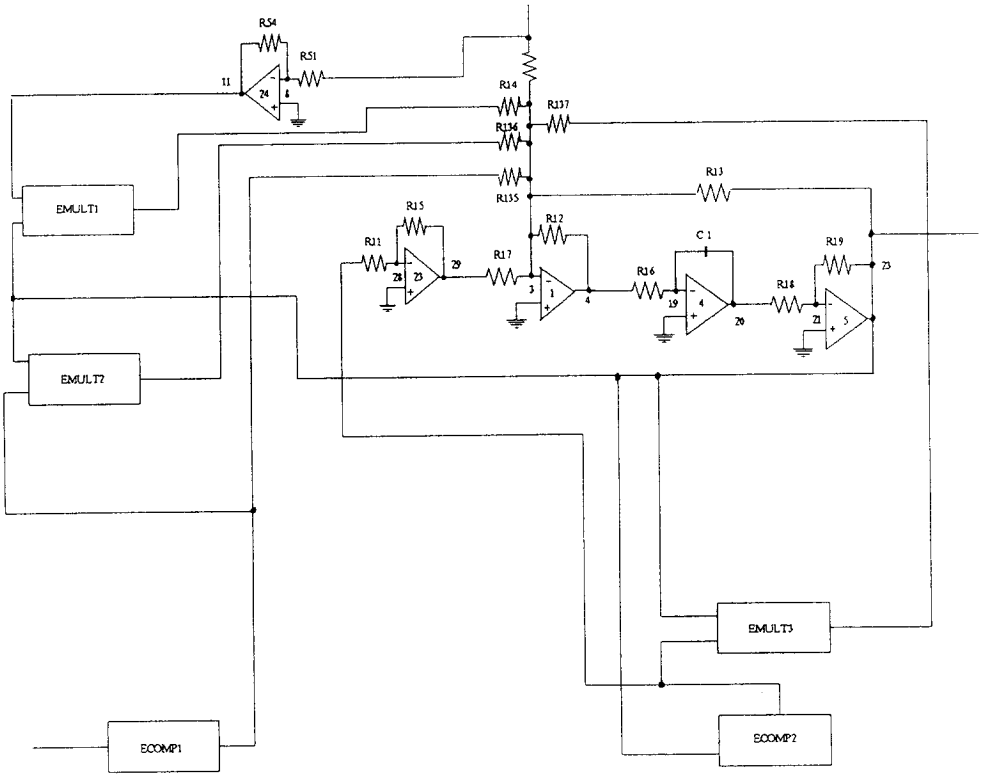


Figure 6. The corresponding analogue behavioural modelling circuit in which the multiplier cell (EMULT) and comparator cell (ECOMP) have been replaced by mathematical functions denoted by the blocks.

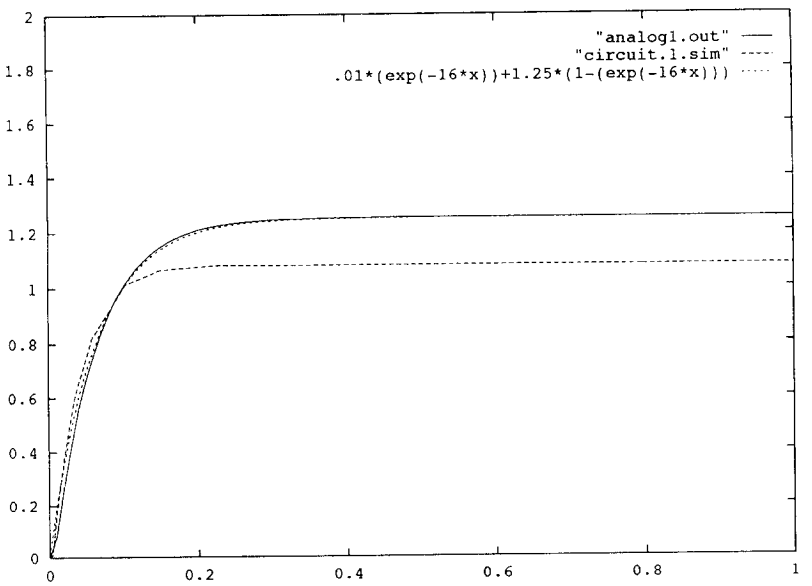


Figure 7. Comparisons of the one-node neural network results simulated from the circuit component modelling (dashed lines), from the analogue behavioural modelling (solid line), and from the exact differential equations (dotted lines).

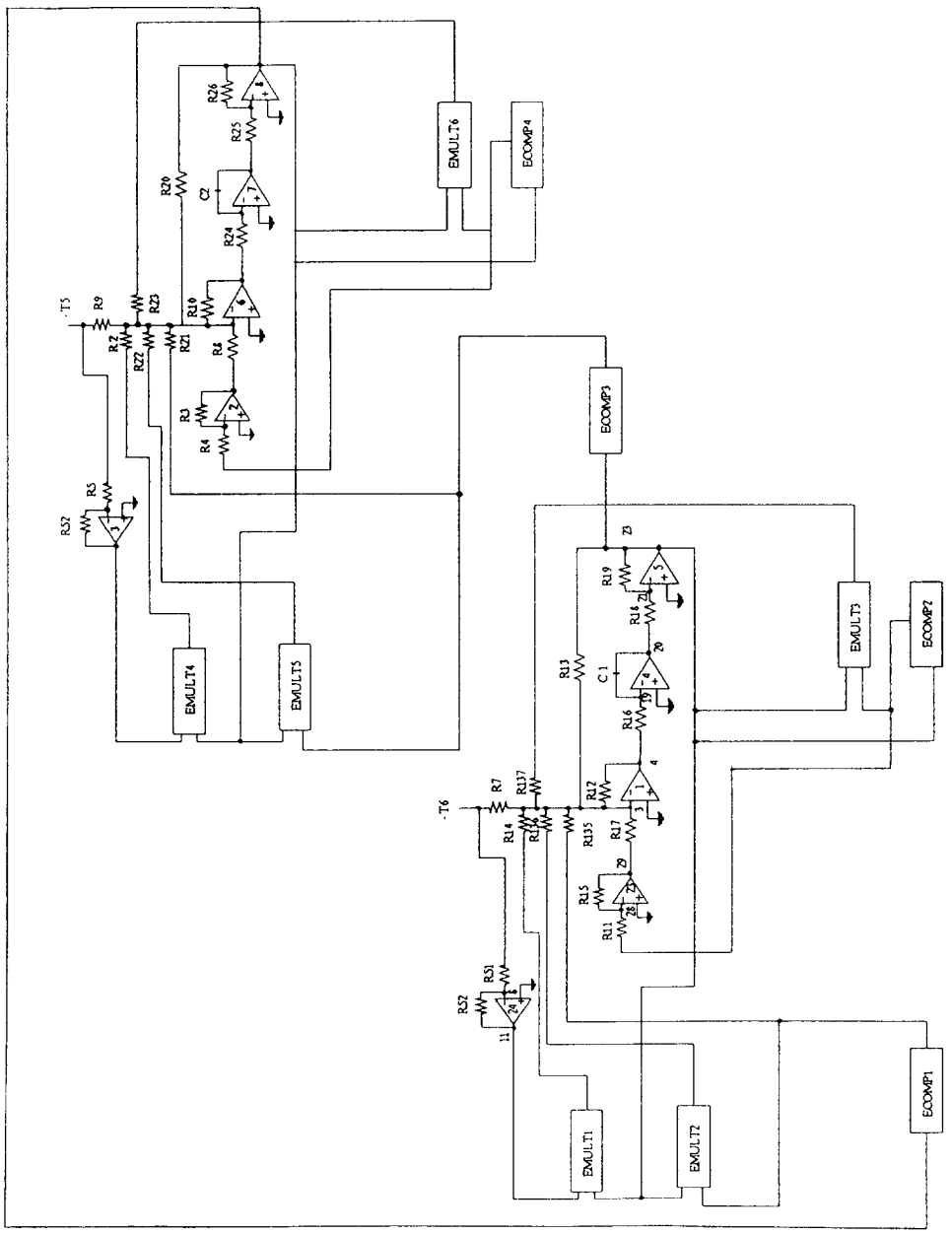


Figure 8. A two-node ART1 neural network constructed using the one-node circuit developed.

circuit developed, as shown in Fig. 8. Simulation results for such a larger ART1 neural network will be reported in a future paper.

4. Summary

An analogue circuit implementation of an adaptive resonance theory (ART1) neural network is presented. The circuit, which performs the same functionality as the one-node neural network in the F2 layer of ART1, is designed based on a set of coupled differential equations and on analogue electronic components such as operational amplifiers. To verify the circuits, computer simulations are carried using Pspice run on a Sun SPARC II workstation. Two different methods are used in simulations; the first method simulates the circuit components using the exact models given in the Pspice library, and the other method describes the circuit component behaviour using mathematical functions. The latter method is more idealistic but requires much less simulation time compared with the first method. Good agreement is found between the circuit simulation results and the exact solutions calculated directly from the differential equations. The one-node circuit developed can be used as a subcircuit for a larger ART1 neural network with an arbitrary number of nodes. This study has thus successfully demonstrated in principle that the ART neural network can be implemented by analogue integrated circuits with conventional electronic components like operational amplifiers.

ACKNOWLEDGMENT

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